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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of

DAVID L. LARKIN

Serial No. 09/988,651 (TI-23422.1)

Filed November 20, 2001

For: A METHOD FOR DECREASING CHC DEGRADATION

Art Unit 2825

Examiner Igwe U. Anya

Customer No. 23494

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11-20-04

Jay M. Cantor, Reg. No. 19,906

BRIEF ON APPEAL

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, a Delaware corporation with offices at 7839 Churchill Way, Dallas, Texas 75251.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals and/or interferences.

STATUS OF CLAIMS

This is an appeal of claims 12 to 29, all of the rejected claims. No claims have been allowed Please charge any costs to Deposit Account No. 20-0668.

STATUS OF AMENDMENTS

An amendment was filed after final rejection and was entered for purposes of appeal.

SUMMARY OF INVENTION

The invention relates to a semiconductor device manufactured using the process of (page 4, lines 5 to 11) providing a semiconductor device having at least one metal layer completed and then providing a hydrogen treatment until hydrogen diffuses *throughout* the semiconductor device. A planarizing dielectric layer can be applied on top of the semiconductor device. The hydrogen treatment can include heating the semiconductor device in a hydrogen rich environment or applying hydrogen in situ by introducing hydrogen as a plasma to the semiconductor device. The planarizing dielectric layer can include a first layer of TEOS, a second layer of HSQ, and a third layer of TEOS or a first layer of TEOS applied by PECVD or a second layer of HSQ applied by coating applied over a first layer of dielectric material or a third layer of TEOS applied by PECVD applied over two layer of dielectric material. The semiconductor device can undergo an N_2 bake after an HSQ layer of a multilayer planarizing dielectric layer is added or the hydrogen treatment after a final layer of the planarizing dielectric layer is added.

ISSUES

The issues on appeal are as follows:

1. Whether claims 12, 14 to 18, 20 and 21 are anticipated by Chen et al. (U.S. 5,866,945) under 35 U.S.C. 102(b).

2. Whether claims 10 to 13 and 20 are anticipated by Fukuda et al. (JP 4,070,74167) under 35 U.S.C. 102(b).

3. Whether claims 12 to 20 and 22 to 29 are unpatentable on the grounds of double patenting over claims 1 to 9 of Patent No. 6,350,673).

4. Whether claims 13 and 19 are patentable over Chen et al. under 35 U.S.C. 103(a).

5. Whether claim 14 is patentable over Fukuda et al. under 35 U.S.C. 103(a).

GROUPING OF CLAIMS

The dependent claims stand or fall together with the claims from which they depend.

ARGUMENT

ISSUE 1

Claims 12, 14 to 18, 20 and 21 were rejected under 35 U.S.C. 102(b) as being anticipated by Chen al. (U.S. 5,866,945). The rejection is without merit.

It is respectfully submitted that applicant can swear back of Chen et al., if necessary, however this has not been done since Chen et al. fails as a proper reference as is demonstrated hereinbelow.

Claim 12 requires, among other steps, providing a semiconductor device having at least one metal layer completed, then applying a planarizing dielectric layer on top of the semiconductor device and then providing a hydrogen treatment until hydrogen diffuses throughout the semiconductor device. No such steps are taught or suggested by Chen et al. As stated at page 9, lines 10ff, "an H_2 bake is done until H_2 completely saturates and protects semiconductor device 10". The method of the present invention provides a device which prevents or minimizes CHC degradation by preventing contaminants from causing such degradation. It is apparent that Chen et al. not only does not recognize the fact that degradation can be caused by contaminants, but, in addition, Chen et al. nowhere teach or

suggest that the entire semiconductor device be treated with the hydrogen diffusion to alleviate this problem. It follows that neither the above noted step nor the combination of steps as claimed are taught or even suggested by Chen et al.

The gratuitous statement by the Examiner in the Advisory Action to the extent that " (1) Fukuda teaches diffusion (sic) of hydrogen through out (sic) the semiconductor device" and that "(2) Chen et al.. do not have a hydrogen on semiconductor, therefore it is inherent hydrogen diffuses through out (sic) thesemiconductor (sic) device upon heating in a nitrogen atmosphere" are not supported by the disclosures of either reference. To begin with, there is no reason for either Fukuda (which is not cited in connection with this rejection) or Chen et al. to cause hydrogen to diffuse throughout the semiconductor device. Neither reference states such result and the basis for the Examiner's statement is incorrect. Hydrogen diffusion throughout the device will take place only if diffusion is carried on for a sufficient length of time to achieve such result. In the manufacturing process, the additional time would increase costs due to slow down of processing time and would not be a part of a process unless required. It follows that there is no basis for the allegation of the Examiner with regard to Chen et al. as stated in the Advisory Action unless specifically so stated.

Claim 14 to 18 and 20 depend from claim 12 and therefore define patentably over Chen et al. for at least the reasons presented above with reference to claim 12.

Claim 21 contains the same feature discussed above with reference to claim 12 and is broader. Accordingly, the arguments presented above with reference to claim 12 apply as well to this claim.

ISSUE 2

Claims 10 to 13 and 20 were rejected under 35 U.S.C. 102(b) as being anticipated by Fukuda et al. (JP 407074167). The rejection is without merit.

The rejection of claims 10 and 11 is not understood since these claims were previously cancelled and is now apparently noted as an erroneous rejection.

With reference to claim 12, in addition to the arguments previously presented, which are repeated and incorporated by reference, the argument presented above also apply since Fukuda et al. also fails as a proper reference as to the invention claimed for the same reasons as set forth above with reference to Chen et al.

Claims 13 and 20 depend from claim 12 and therefore define patentably over Fukuda et al. for at least the reasons presented above with reference to claim 12.

ISSUE 3

With reference to the rejection of claims 22 to 29 on the ground of double patenting has apparently been withdrawn. It is respectfully submitted that there was a requirement for restriction in the parent application between claims 1 to 9 and claims 10 to 20, claims 21 to 29 claiming the same invention as claims 12 to 20 except for the omission of one of the steps which relates to a feature nowhere taught or suggested by the prior art as demonstrated above. The basis for the requirement for restriction appears to be upon the preamble in view of the position taken by the examiner in this application and presumably in the prior application. Accordingly, since the preamble in all of the claims in this application is the same, all of the claims of this application must be to the same invention which is different

from the invention claimed in the parent application in which the requirement for restriction was made. Accordingly, in view of 35 U.S.C. § 121, this rejection is improper and therefore respectfully traversed.

ISSUE 4

Claims 13 and 19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. The rejection is without merit.

Claims 13 and 19 depend from claim 12 and therefore define patentably over Chen et al. for at least the reasons presented above with reference to claim 12.

ISSUE 5

Claim 14 was rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuda in view of Wuu et al. (U.S. 5,796,150). The rejection is without merit.

Claim 14 depends from claim 12 and therefore defines patentably over the applied references for at least the reasons presented above with reference to claim 12 since Wuu et al. fails to overcome the deficiencies in Fukuda et al. as noted above.

Claims 22 to 29 have not been rejected other than for double patenting, the basis of which was improper as noted above. Since this rejection has been withdrawn as to claims 22 to 29, these claims must therefore be assumed to be allowed.

CONCLUSIONS

For the reasons stated above, reversal of the final rejection and allowance of the claims on appeal is requested that justice be done in the premises.

Respectfully submitted,

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APPENDIX

The claims on appeal read as follows:

12. A semiconductor device manufactured using the following process:

providing a semiconductor device having at least one metal layer completed;

then applying a planarizing dielectric layer on top of the semiconductor device; and

then providing a hydrogen treatment until hydrogen diffuses throughout the semiconductor device.

13. The semiconductor device of Claim 12, wherein the hydrogen treatment includes heating the semiconductor device in a hydrogen rich environment.

14. The semiconductor device of Claim 12, wherein the hydrogen treatment includes applying hydrogen in situ by introducing hydrogen as a plasma to the semiconductor device.

15. The semiconductor device of Claim 12, wherein the planarizing dielectric layer includes a first layer of TEOS, a second layer of HSQ, and a third layer of TEOS.

16. The semiconductor device of Claim 12, wherein the planarizing dielectric layer includes a first layer of TEOS applied by PECVD.

17. The semiconductor device of Claim 12, wherein the planarizing dielectric layer includes a second layer of HSQ applied by coating applied over a first layer of dielectric material.

18. The semiconductor device of Claim 12, wherein the planarizing dielectric layer includes a third layer of TEOS applied by PECVD applied over two layer of dielectric material.

19. The semiconductor device of Claim 12, wherein the semiconductor device undergoes an N_2 bake after an HSQ layer of a multilayer planarizing dielectric layer is added.

20. The semiconductor device of Claim 12, wherein the semiconductor device undergoes the hydrogen treatment after a final layer of the planarizing dielectric layer is added.

21. A semiconductor device manufactured using the following process:

providing a semiconductor device having thereon at least one metal layer completed; and

then providing a hydrogen treatment until hydrogen diffuses throughout the semiconductor device.

22. The semiconductor device of Claim 21 wherein the hydrogen treatment includes heating the semiconductor device in a hydrogen rich environment.

23. The semiconductor device of Claim 21 wherein the hydrogen treatment includes applying hydrogen in situ by introducing hydrogen as a plasma to the semiconductor device.

24. The semiconductor device of Claim 21, wherein the planarizing dielectric layer includes a first layer of TEOS, a second layer of HSQ, and a third layer of TEOS.

25. The semiconductor device of Claim 21, wherein the planarizing dielectric layer includes a first layer of TEOS applied by PECVD.

26. The semiconductor device of Claim 21, wherein the planarizing dielectric layer includes a second layer of HSQ applied by coating applied over a first layer of dielectric material.

27. The semiconductor device of Claim 21, wherein the planarizing dielectric layer includes a third layer of TEOS applied by PECVD applied over two layer of dielectric material.

28. The semiconductor device of Claim 21, wherein the semiconductor device undergoes an N_2 bake after an HSQ layer of a multilayer planarizing dielectric layer is added.

29. The semiconductor device of Claim 21, wherein the semiconductor device undergoes the hydrogen treatment after a final layer of the planarizing dielectric layer is added.